CLAIMS

What is claimed is:

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1	1	A computer system,	COMMERCING
1		A COMBUICI SYSTEM.	COHIDHSHIE.
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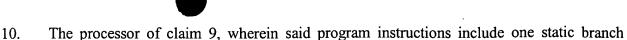
- 2 a processor which includes a hardware branch predictor; and
- a program of software instructions executed by said processor, said software instructions
- 4 including conditional branch instructions and separate static branch prediction instructions;
- said static branch prediction instructions include static branch prediction bits which
- 6 correspond to conditional branch instructions.
- 1 2. The computer system of claim 1, wherein said program includes one static branch
- 2 prediction instruction for each group of n other instructions.
- 1 3. The computer system of claim 2, wherein n is 7.
- 1 4. The computer system of claim 2, wherein said static branch prediction bits included in a
- 2 static branch prediction instruction include pairs of prediction bits, each pair providing prediction
- 3 information for a separate instruction in said group of n other instructions.
- 1 5. The computer system of claim 4 wherein said prediction information includes a member
- 2 selected from the group consisting of: do not use static prediction, predict taken, and predict not
- 3 taken.



- 1 6. The computer system of claim 4 wherein each pair of prediction bits corresponds to another
- 2 instruction and each pair of prediction bits is encoded as: 00 and 01 mean do not use static
- 3 prediction, 10 means predict taken and 11 means predict not taken.
- 1 7. The computer system of claim 1 wherein said static branch prediction bits include static
- 2 branch prediction information that includes encoded information directing the processor to ignore
- 3 the predictions supplied by the hardware branch predictor.
- 1 8. The computer system of claim 1 wherein said hardware branch predictor includes a log in
- which the results of all executed conditional branch instructions are stored.
- 1 9. A processor, comprising:
- 2 fetch logic that fetches program instructions from a source external to said processor;
- a dynamic branch predictor coupled to said fetch logic, said dynamic branch predictor
- 4 supplies predictions regarding conditional branch instructions to said fetch logic;
- an instruction queue coupled to said dynamic predictor, said fetch logic storing fetched
- 6 instructions in said instruction; and
- an execution unit coupled to said instruction queue and executing instructions provided
- 8 from said instruction queue;
- 9 said fetch logic examines fetched instructions for a predetermined register identifier that
- 10 identifies that instruction as a static branch prediction instruction that provides static branch
- prediction information about other fetched instructions.

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- 2 prediction instruction for each group of n other instructions.
- 1 11. The processor of claim 10, wherein n is 7.
- 1 12. The computer system of claim 10, wherein said static branch prediction bits included in a
- 2 static branch prediction instruction include a plurality of pairs of prediction bits, each pair
- 3 providing prediction information for a separate instruction in said group of n other instructions.
- 1 13. The processor of claim 12 wherein said prediction information includes a member selected
- 2 from the group consisting of: do not use static prediction, predict taken, and predict not taken.
- 1 14. The processor of claim 12 wherein each pair of prediction bits corresponds to another
- 2 instruction and each pair of prediction bits is encoded by said fetch logic as: 00 and 01 mean do not
- 3 use static prediction, 10 means predict taken and 11 means predict not taken.
- 1 15. The processor of claim 9 wherein said static branch prediction instruction includes branch
- 2 prediction bits which encodes information directing said fetch logic to ignore the predictions
- 3 supplied by the dynamic branch predictor.
- 1 16. The processor of claim 9 wherein said dynamic branch predictor includes a log in which
- 2 the results of all executed conditional branch instructions are stored.





- 1 17. The processor of claim 9 wherein said predetermined identifier comprises a register
- 2 identifier.
- 1 18. A method of predicting the outcome of conditional branch instructions, comprising:
- 2 (a) including a static branch predictor software instruction in a program, said branch
- 3 prediction software instruction including branch prediction information pertaining to other
- 4 instructions in the program;
- 5 (b) fetching said branch prediction software instructions;
- 6 (c) decoding said branch prediction software instructions to determine if said decoded
- 7 instruction is a branch prediction software instruction; and
- 8 (d) if said decoded instruction is a branch prediction software instruction, then using
- 9 said branch prediction information for branch prediction.
- 1 19. The method of claim 18 wherein (a) comprises including a branch prediction software
- 2 instruction corresponding to a predetermined group of other instructions.
- 1 20. The method of claim 19 wherein said group includes 7 instructions.
- 1 21. The method of claim 18 wherein said branch prediction information includes pairs of bits,
- 2 each pair corresponding to one of said other instructions.





- 1 22. The method of claim 21 further including decoding said pairs of bits to determine whether,
- 2 for said other instruction corresponding to said pair, said other instruction is predicted taken,
- 3 predicted not taken or no static branch prediction is provided.

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